STI POLISH ENHANCEMENT USING FIXED ABRASIVES WITH AMINO ACID ADDITIVES

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention generally relate to planarization of semiconductor devices and to methods and compositions for material removal using polishing techniques.

Description of the Related Art

[0002] The semiconductor industry's progress to globally planarize topographical features with diverse pattern densities commonly used in the manufacture of high performance very large scale integration (VLSI) and ultra large-scale integration (ULSI) devices has pushed semiconductor performance ever faster. As the fringes of circuit technology are pressed, the shrinking dimensions of interconnects in sub-half micron and smaller features for the next generation of VLSI and ULSI technologies has placed additional demands on the processing capabilities. Structures with increasingly smaller device dimensions, high aspect ratio features, denser packaging arrangements, and higher metal-insulator wiring levels demand stringent planarity requirements. The multilevel interconnects that lie at the heart of semiconductor technology require precise processing of high aspect ratio features, such as vias, contacts, lines, and other interconnects. Reliable formation of these interconnects is important to VLSI and ULSI success, and to the continued effort to increase circuit density and quality of individual substrates and die.

[0003] Multilevel interconnects are formed by the sequential deposition and removal of materials from the substrate surface to form conductive interconnect features. As layers of materials are sequentially deposited and removed, the uppermost surface of the substrate may become non-planar across its surface and require planarization. Planarizing, or "polishing" a surface, is a process where material is removed from the

substrate surface to form a generally even, planar surface. Planarization is useful in damascene processes to remove excess deposited material and to provide an even surface for subsequent levels of metallization and processing. Planarization may also be used to remove undesired surface topography and surface defects, such as rough surfaces, agglomerated materials, crystal lattice damage, scratches, and contaminated layers or materials.

[0004] Chemical mechanical planarization, or chemical mechanical polishing (CMP), is a common technique used to planarize substrates. CMP utilizes two modes to planarize substrates. One mode is a chemical reaction using a chemical composition, typically a slurry or other fluid medium, for removal of material from substrates, and the other is mechanical force. In conventional CMP techniques, a substrate carrier or polishing head is mounted on a carrier assembly and positioned in contact with a polishing pad in a CMP apparatus. The carrier assembly provides a controllable pressure to the substrate urging the substrate against the polishing pad. The pad is moved relative to the substrate by an external driving force. Thus, the CMP apparatus effects a polishing or rubbing movement between the substrate surface and the polishing pad, while dispensing a polishing composition to encompass both chemical and mechanical activities.

[0005] CMP may be used in the fabrication of shallow trench isolation (STI) structures. STI has rapidly become the premier technique for isolation in complementary metal-oxide-semiconductor (CMOS) field-effect transistor devices, owing to the fact that feature sizes can be made very small to provide higher device density. STI in combination with CMP has been proposed to replace the local oxidation of silicon (LOCOS) technology for sub-half micron devices to enhance performance and improve manufacturability. STI structures are used to separate transistors and components of a transistor, such as source/drain junctions or channel stops on a substrate surface during fabrication. STI structures can be formed by deposition of a series of dielectric materials, followed by polishing the substrate surface to remove excess or undesired dielectric materials.

[0006] Figure 1 shows an example of one stage of the STI formation process, which includes depositing a silicon nitride layer 20 on an oxide layer 15 formed on the surface of a substrate 10, patterning and etching the substrate surface to form a feature definition 35, and depositing a silicon oxide material 30 in sufficient amounts to fill the feature definitions 35, resulting in oxide overfill 72 and high density plasma (HDP) peaks 70 on the substrate surface. Overfill is defined herein as the total thickness of the oxide layer over the active-area nitride minus the step height. A STI patterning and etching process generally involves a photoresist used to define shallow trench isolation on silicon nitride-oxide layers. The layers are then dry-etched using a reactive ion etch (RIE) technique, for example, to define trenches and shallow trench isolation structures. The trenches are typically filled with silicon oxide material 30 by a technique, such as high-density plasma chemical vapor deposition (HDP-CVD). The silicon nitride layer 20 may perform as a hard mask during RIE etching of the features in the substrate and/or as a polishing stop during subsequent polishing processes. Polishing the substrate surface is typically engaged as the next step to remove these HDP peaks 70 and excess silicon oxide material 30. Such STI fabrication processes require polishing of the silicon oxide material 30 to the silicon nitride layer 20 with a minimal removal of silicon nitride during the polishing process in order to prevent damaging of the underlying materials, such as the oxide layer 15 and the doped silicon substrate 10.

[0007] The STI substrate is typically polished using conventional CMP processes, which are performed with conventional polishing pads and abrasive articles, such as a polishing composition or slurry containing abrasive particles in a reactive solution. Conventional polishing pads are typically made out of foam resin, such as urethane and polyurethane, to expose a grooved porous polymeric surface. The abrasive slurry employed with a conventional polishing pad is varied in accordance with the particular material undergoing polishing. During CMP processes, the abrasive slurry is in contact with the pores and grooves of the polymeric surface to convey the abrasive slurry to the substrate undergoing polishing. Generally, a polishing pad of choice can be selected according to its physical properties, such as pore density, microstructures, and compressibility of the pad surface, for example.

[0008] However, STI polishing processes using conventional polishing pads and abrasive slurries have been observed to result in overpolishing of the deposited surface and formation of recesses in the STI features and other topographical defects, such as microscratches on the deposited surface. This phenomenon of overpolishing and forming recesses in the STI features is referred to as dishing. Dishing is highly undesirable because dishing of substrate features may detrimentally affect device fabrication by causing failure of isolation of transistors and transistor components from one another resulting in short-circuits.

[0009] Figure 2A is a schematic diagram illustrating the phenomena of dishing observed when polishing with conventional techniques. During polishing of the silicon oxide material 30 to the silicon nitride layer 20, the silicon oxide material 30 may be overpolished and surface defects, such as recesses 55, may be formed in the silicon oxide material 30. The excess amount of silicon oxide material removed as a result of overpolishing the substrate surface, represented by dashed lines, is considered the amount of dishing 50 of the feature.

[0010] In addition to dishing, conventional polishing techniques can result in silicon nitride loss due to excess polishing, as illustrated in Figure 2B. Silicon nitride loss may take the form of excess removal of silicon nitride, or "thinning" of the silicon nitride layer, from the desired amount 60 of silicon nitride. The silicon nitride loss may render the silicon nitride layer 30 unable to prevent or limit damage due to contamination of the substrate material, nor to prevent overpolish of the feature definitions 35 (oxide isolation), during polishing or subsequent processing.

[0011] Minimal removal of the silicon nitride layer 20 prevents overpolish or dishing of the trenches of the silicon oxide-filled feature definitions 35, which can lead to a phenomenon known as polysilicon wrap-around. Figures 3A and 3B are schematic diagrams illustrating the phenomenon of polysilicon wrap-around of a STI structure which includes a deposited gate polysilicon film 90 disposed on top of a substrate 10, generally employed for transistor gate fabrication, a feature definition 35 filed with a silicon oxide material 30, and a device active region 40 with an oxide material 15

between the deposited gate polysilicon film 90 and the device active regions 40. In a typical STI fabrication sequence, the wafer is subjected to one or more hydrofluoric acid (HF) "deglazing" steps after completion of the CMP process to remove excess silicon oxide material 30 and before fabrication of the transistor gate electrodes. Hydrofluoric acid exposure removes the silicon nitride material 20 and can significantly reduce the thickness of the oxide-filled feature definitions 35.

[0012] Figure 3A is a cross-sectional profile of a properly fabricated STI structure, where the silicon nitride material 20 has been removed by hydrofluoric acid deglazing and a gate polysilicon film 90 is then deposited. In Figure 3A, the top surface 92 of the silicon oxide-filled feature definition 35 is in a relatively higher planar position than the top surface 96 of the device active region 40. The gate polysilicon film 90 deposited during transistor gate fabrication exhibits a smooth upward transition 91 from the device active regions 40 of the substrate 10 to the top surface 92 of the silicon oxide-filed feature definition 35 of the substrate 10. Figure 3B is a cross section of an improperly fabricated STI structure in which the top surface 94 of the silicon oxide-filed feature definition 35 is in a relatively lower planar position than the top surface 98 of the device active region 40. The downward transition 93 in the gate polysilicon film 90 over the corner of the device active regions 40 and the silicon oxide-filled feature definition 35 is known as gate wrap-around or polysilicon wrap-around, and thus creates a transistor with a parasitic edge 95 with a lower threshold voltage (V_t) than an active device.

[0013] One solution to limit dishing of substrate features is to polish a substrate surface using a fixed abrasive polishing pad and a CMP composition or slurry that does not contain abrasive particles. A fixed abrasive polishing pad contains fixed abrasive particles held in a containment media such as a backing sheet, which provide mechanical activity to the substrate surface, along with a plurality of geometric abrasive composite elements adhered to the containment media.

[0014] CMP processes using fixed abrasive polishing pads have demonstrated a removal rate selectivity of an oxide layer to a nitride layer close to 1:1, and oxide dishing is typically much lower than that observed with conventional abrasive slurry

processes. Once the oxide has cleared, however, continued polishing erodes away the nitride layer. Dishing, within-wafer non-uniformity (WIWNU) and within-die non-uniformity (WIDNU) are all functions of overpolish, and all increase as the loss of the nitride layer increases. This behavior makes it difficult to polish wafers with large variations in pattern density. The oxide film over small, isolated nitride features tends to clear much faster than that over large nitride features, leading to significant nitride erosion at the small features as well as significant increases in WIDNU.

[0015] Fixed abrasive (FA) CMP technology is gaining market acceptance in dynamic random access memory (DRAM) manufacturing for the direct planarization of STI structures. The salient feature of FA CMP is its extremely high selectivity to topography whereby high areas on a patterned silicon wafer are polished away much faster than low areas, and the polishing removal rate decreases dramatically as the wafer approaches planarity. DRAM applications can take advantage of the selectivity to topography ("stop-on-planar" capability) offered by FA technology because they typically have a limited number of feature sizes and densities in the circuit design.

[0016] In contrast, fixed abrasive CMP is having more difficulty penetrating the logic STI market. Logic applications, which may include a range of feature sizes and densities, require selectivity to film type ("stop-on-nitride" capability) to prevent excessive erosion of small nitride features during the overpolish time required to clear the larger features. Fixed abrasive CMP has been observed to excessively polish the underlying silicon nitride layer of STI substrates when polishing silicon oxide layers. The excessive nitride polishing or the absence of "stop-on-nitride" capability results in nitride loss which exposes the underlying silicon to damage from polishing or chemical activity, or to trench oxide loss resulting in gate wrap-around, which detrimentally affects device quality and performance. In addition, it is difficult to polish wafers with large oxide overfills once the topography has been planarized ("stop-on-planar" capability).

[0017] Therefore, there exists a need for a method and related polishing apparatus, which facilitates the removal of dielectric materials with minimal or reduced dishing and minimal or reduced loss of underlying materials.

SUMMARY OF THE INVENTION

[0018] Embodiments of the invention generally provide methods and compositions for planarizing a substrate surface with selective removal rates and low dishing. In one aspect, a method is provided for selectively removing a dielectric from a substrate having at least a first and a second dielectric material disposed thereon. The method includes positioning the substrate in proximity with a fixed abrasive polishing pad, dispensing a polishing composition having at least one organic compound between the substrate and the polishing pad, and chemical mechanical polishing the substrate. In one embodiment, the first dielectric material is removed at a higher removal rate than the second dielectric material. In one embodiment, the polishing composition is abrasive free.

[0019] In another aspect, a method is provided for processing a substrate having an oxide material disposed on a nitride material. The method includes positioning the substrate in proximity with a fixed abrasive polishing pad, dispensing a polishing composition having at least one organic compound, at least one pH adjusting agent, and deionized water, between the substrate and the polishing pad, and removing the oxide material and nitride material at a removal rate ratio of the oxide material to the nitride material between about 10:1 or greater.

[0020] In another aspect, the invention provides a composition for removing dielectric materials in a chemical mechanical polishing technique. In one embodiment, the composition is abrasive-free and/or may be an additive to an abrasive-free slurry. In another embodiment, the chemical mechanical polishing technique uses a fixed abrasive polishing pad. Illustratively, the composition includes at least one organic compound selected from a group of amino acids, at least one pH adjusting agent, and deionized water.

[0021] Another aspect of the invention provides a system for selectively removing dielectric material disposed on a substrate, wherein the substrate has at least a first and a second dielectric material disposed thereon. The system includes a polishing platen having a fixed abrasive polishing pad disposed thereon and in proximity with the substrate for polishing the substrate, and a microprocessor based controller. The microprocessor based controller is configured to cause the system to contact the substrate, to deliver to the substrate a polishing composition having at least one organic compound therein such that the polishing composition is in contact with the substrate and the fixed abrasive polishing pad, and to remove the first dielectric material at a higher removal rate than the second dielectric material.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] So that the manner in which the features of the invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof, which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0023] Figure 1 shows an example of one stage of the STI formation process.

[0024] Figures 2A and 2B are schematic diagrams illustrating the phenomena of dishing and nitride loss of a STI structure.

[0025] Figures 3A and 3B are schematic diagrams illustrating the phenomena of polysilicon wrap-around of a STI structure.

[0026] Figure 4 is a schematic view of a chemical mechanical polishing apparatus.

[0027] Figure 5 is a flow chart illustrating the processing steps according to one embodiment of the invention.

[0028] Figures 6A and 6B are schematic diagrams illustrating one embodiment of polishing a substrate by the methods described herein.

[0029] Figures 7A-7C are graphs illustrating removal rates for silicon oxide and silicon nitride, and silicon oxide to silicon nitride selectivity on blanket wafers.

[0030] Figures 8A-8E are graphs illustrating overpolish comparison of patterned DRAM wafers.

[0031] Figures 9A-9D are graphs illustrating the remaining thickness profile of patterned DRAM wafers.

[0032] Figures 10A and 10B are graphs illustrating the remaining thickness profile of logic-type wafers.

DETAILED DESCRIPTION OF THE INVENTION

[0033] Embodiments of the invention will be described below in reference to a planarizing process and composition that can be carried out using chemical mechanical polishing process equipment, such as a Reflexion™ CMP System available from Applied Materials, Inc., of Santa Clara, California. In addition, any system enabling chemical mechanical polishing using the methods or compositions described herein can be used to advantage. Examples of other suitable polishing apparatuses include an Obsidian™ 8200C system and a Mirra® CMP System available from Applied Materials, Incorporated. The following apparatus description is illustrative and should not be construed or interpreted as limiting the scope of the invention.

[0034] Figure 4 is a schematic view of a CMP apparatus 100. The CMP apparatus 100 generally includes a polishing head 102, a polishing platen 108 and a polishing pad 106 disposed on the polishing platen 108. The polishing head 102 is capable of holding a substrate 112 thereon. The polishing platen 108 may be a linear web, a linear belt platen, or a rotatable platen. CMP systems may further include a carousel, at least one polishing head assembly 104 suspended from the carousel to hold the polishing head 102, and a positioning member coupled to the carousel to move the carousel and position the polishing head assembly 104 over the platen. The polishing head assembly 104 provides a controllable pressure 110 to the substrate 112 urging the substrate 112 against the polishing pad 106. One example of the polishing pad 106

that may be used herein is a fixed abrasive polishing pad such as a M3100 SlurryFree™ CMP Fixed Abrasive Pad from 3M of St. Paul, Minnesota, which uses cerium oxide as abrasive articles.

[0035] The CMP apparatus 100 effects a polishing or rubbing movement between the surface of the substrate 112 and the polishing pad 106 by applying an external force 116 between them either linearly or in rotationally while dispensing a polishing composition 118 or slurry with or without abrasive particles in order to effect both chemical and mechanical activities.

Chemical Mechanical Polishing Process and Composition.

[0036] Embodiments of the invention include CMP processes and compositions comprised of organic compounds such as amino acids. In one aspect, a method of processing a substrate having an oxide material disposed on a nitride material is provided. The method includes positioning the substrate in proximity with a fixed abrasive polishing pad, dispensing a polishing composition between the substrate and the polishing pad, and removing the oxide material at a higher removal rate than the nitride material. Polishing compositions containing organic compounds in combination with fixed abrasive polishing pads enable modification of the removal rates for polishing different dielectric materials and reduce dishing and loss of adjacent layers. The organic compounds in the polishing compositions are believed to provide "stop-on-nitride" capability to existing "stop-on-planar" capability of chemical mechanical polishing using fixed abrasive polishing pads.

[0037] In another aspect, the invention provides a chemical mechanical polishing composition for removing dielectric materials, including at least one organic compound, at least one pH adjusting agent, deionized water, and optionally a disperser. The addition of organic compounds to the polishing composition widens the fixed abrasive process window, improves DRAM polishing performance, and enables chemical mechanical polishing using fixed abrasive polishing pads for logic applications.

[0038] Figure 5 is a flow chart illustrating one embodiment of a process for planarizing a substrate surface. A method 200 of planarizing a substrate surface using

a fixed abrasive polishing pad and a polishing composition containing at least one organic compound is provided. A substrate having at least a first and a second dielectric material deposited thereon is positioned in a polishing apparatus having a fixed abrasive polishing pad at Step 210. At Step 220, a polishing composition, containing at least one organic compound such as glycine, is applied to the fixed abrasive polishing pad disposed on the polishing apparatus, wherein the at least one organic compound in the polishing composition modifies the removal rates of one or more dielectric materials. The substrate and the fixed abrasive polishing pad are contacted and one or more dielectric materials are removed from the substrate surface at a higher removal rate than the other dielectric materials at Step 230.

[0039] As used herein "substrate" refers to the object being polished and may include, for example, a silicon based material having materials disposed thereon. The substrates that may be polished by Step 210 include shallow trench isolation structures formed in a series of dielectric layers, such as silicon oxide and silicon nitride. The invention contemplates chemical mechanical polishing of dielectric materials conventionally employed in the manufacture of semiconductor devices, for example, silicon dioxide, silicon nitride, silicon oxy-nitride, phosphorus-doped silicon glass (PSG), boron-doped silicon glass (BSG), boron-phosphorus-doped silicon glass (BPSG), silicon dioxide derived from tetraethyl orthosilicate (TEOS), and silane, which are deposited by various chemical vapor deposition (CVD) techniques, and combinations thereof.

[0040] The polishing composition delivered to the fixed abrasive polishing pad at Step 220 may include at least one organic compound present in an amount between about 0.01 weight percentage (wt. %) and about 20 wt. % of the polishing composition. A concentration of organic compounds between about 0.01 wt. % and about 8 wt. % is preferably used in the polishing composition. Most preferably, the at least one organic compound may comprise between about 1 wt. % and about 6 wt. % of the composition. The polishing composition may be delivered or supplied to the fixed abrasive polishing pad at a flow rate of, for example, between about 5 ml/min and about 500 ml/min from a storage medium disposed in or near the CMP system.

[0041] Organic compounds useful in the composition include those which may selectively modify the removal rate of one or more dielectric materials in relation to other dielectric materials. In one embodiment, the organic compounds are selected to result in a higher removal rate for silicon oxide material than that for silicon nitride material. Examples of organic compounds include amino acids having amino (NH_2-) and carboxyl (-COOH) terminal ends, and derivatives thereof, such as glycine, proline, arginine, lysine, and combinations thereof.

[0042] The polishing composition may also include at least one pH adjusting agent to adjust the pH of the polishing composition to improve polishing performance, such as by allowing a positive or negative charge to be developed on one or more material disposed on a substrate surface and attract the appropriately charged organic amino acid compounds. The at least one pH adjusting agent in the composition may be added to adjust the pH level of the composition to about 7 or more. For example, a pH-adjusting agent may be added to the composition in an amount sufficient to produce a basic pH, *i.e.*, a pH between about 10 to about 12. The at least one pH adjusting agent may comprise any of various inorganic and/or organic bases, such as potassium hydroxide (KOH) and ammonium hydroxide.

[0043] The at least one pH adjusting agent may serve as a pad lubricant or a coolant and may increase or decrease the hydration of the silicon-based dielectric materials resulting in the formation of silanol (Si-OH) groups, which enhance removal of materials from the substrate surface. The at least one pH adjusting agent also affects selective formation of certain complexes between the polishing composition and one or more surface dielectric materials and thus affects removal rates of different surface dielectric materials. For example, an acidic pH increases the formation of silanol on silicon oxide and increases the ability of the polishing composition to complex with the silicon oxide material but not the silicon nitride material.

[0044] One possible mechanism for the polishing composition to work with FA CMP is that the at least one organic compound may complex with silanol (Si-OH) surface groups of the silicon nitride film and suppress removal of the silicon nitride film.

Another possible mechanism is that the at least one organic compound in the polishing composition modifies the removal rates of the dielectric materials by forming a removal resistant or passivation layer on at least one material on the substrate surface and this modification of removal rates is favored by, in this case, an increasing pH.

[0045] An example of a polishing composition includes between about 4 wt.% and about 8 wt.% of glycine, distilled water, and potassium hydroxide as a pH adjusting agent in a sufficient amount to produce a pH level of about 10.5. A fixed abrasive polishing pad containing ceria-based abrasives in an equivalent concentration between about 1 wt.% and about 50 wt.% of the polishing pad may be used with the polishing composition to remove material from the substrate surface.

[0046] At Step 230, the substrate and the fixed abrasive polishing pad are contacted and one dielectric material is removed at a higher removal rate than the other dielectric material from the substrate surface. The material may be removed at a rate between about 50 Å/min and about 5000 Å/min. In one embodiment, a removal rate ratio, or selectivity, of the first material, such as silicon oxide, to the second material, such as silicon nitride, of about 10:1 or greater may be achieved through the use of the organic compounds in a composition described herein. In another embodiment, a removal rate of first material to second material from about 100:1 or greater to about 1200:1 or greater may be achieved from the processes described herein. However, the removal rates and removal rate ratios can vary with the processing parameters and polishing composition used.

[0047] An example of a polishing process at Step 230 includes moving the polishing pad relative to the substrate at a rate between about 15 rpm and about 200 rpm for a polishing pad disposed on a polishing system. The polishing media is moved relative to the substrate at a rate between about 25 rpm and about 100 rpm for a polishing pad disposed on a round or rotatable platen polishing system. A pressure between about 0.5 psi and about 6.0 psi between the substrate and the polishing pad can be used to provide mechanical activity to the polishing process. Alternatively, the invention

contemplates polishing the substrate on a variety of polishing platens, such as rotatable platens, rotatable linear platens, and orbital polishing platens.

[0048] Figures 6A and 6B illustrate the selective removal of materials from the substrate surface. Figure 6A shows an example of substrate materials deposited for the STI formation process. A thermal oxide layer 515 and silicon nitride layer 520 are disposed and patterned over a silicon substrate (or doped silicon layer) 510. The thermal oxide layer 515, silicon nitride layer 520, and silicon substrate 510 are etched to form feature definitions 535, which are then filled by depositing a silicon oxide material 530. The silicon oxide 530 is then polished using the polishing composition described herein to expose the silicon nitride layer. Polishing is continued and the silicon oxide material 530 is removed while the silicon nitride layer 520 remains substantially unpolished as shown in Figure 6B. Subsequent to ending the polishing process, the silicon nitride layer 520 may be removed prior to further substrate processing.

[0049] Addition of an amino acid such as glycine at the proper concentration and pH vastly enhances the performance and flexibility of fixed abrasive CMP. The silicon oxide removal rate is greatly increased while the silicon nitride removal rate is retarded. This enhancement enables shorter polishing times, increased throughput, polishing of thicker overburden substrates, polishing of substrates with a range of feature sizes and densities (e.g., logic applications), improved within-wafer and within-die uniformities, minimized dishing and silicon nitride loss, improved wafer-to-wafer polishing stability, decreased performance degradation due to overpolish, and improved pad wetting.

Examples:

[0050] An example of a polishing process described herein comprises delivering a polishing composition to a fixed abrasive polishing pad containing ceria abrasive particles at a flow rate between 50 ml/min and about 500 ml/min, the polishing composition including between about 4 wt% and about 8 wt% of glycine, deionized water, and potassium hydroxide as a pH adjusting agent in a sufficient amount to produce a pH level between of about 10.5 and 12. A polishing pressure between about

1 and about 6 psi, and a polishing speed between about 25 rpm and about 100 rpm for a polishing duration between about 30 seconds and about 300 seconds may be used to planarize a substrate.

Example A:

[0051] The following is one example of an improved polishing process for a sample shallow trench isolation structure. The CMP system used is an Obsidian™ 8200C system from Applied Materials Inc. of Santa Clara, California. The fixed abrasive polishing pad used in this case was a 3M M3100 (SWR 159) polishing pad for DRAM applications together with a 3M 6900 subpad. M3100 consists of regularly spaced cylindrical posts formed of cerium oxide abrasive particles in a polymer binder, and requires *in situ* topography for pad activation.

[0052] Experiments were performed on blanket and patterned STI wafers. Since blanket wafers (20,000 Å blanket PETEOS oxide wafers and 1500-Å blanket LPCVD nitride wafers) do not have the microtopography necessary to effectively activate the M3100 pad, the polishing behavior of blanket wafers is substantially different from that of DRAM wafers. However, the relative trends in polishing selectivity seen with blanket wafers apply to patterned wafers also. All wafers were polished with a down force of 4 psi and a speed of 600 mm/s.

[0053] Blanket silicon nitride and silicon oxide wafers were used to investigate the effect of pH and glycine concentration on removal rate and silicon oxide versus silicon nitride selectivity. Glycine concentrations of 0%, 3% and 6% were used at pH levels of 10.5, 11.3, and 12.0. Blanket wafers were polished for 180 seconds. The polishing removal rate results for blanket silicon oxide and silicon nitride wafers using different pH and glycine concentrations are presented in Figure 7A-7C.

[0054] Figure 7A shows the amount of oxide removed versus pH for given glycine concentrations. For the standard process (no glycine addition), the silicon oxide polishing removal rate increases with increasing pH. With the addition of 6% glycine, the silicon oxide polishing removal rate is enhanced and the response is reversed such that the removal rate decreases as pH increases. The responses appear to converge

at higher pH and suggest a decreased glycine effect. At a relatively lower pH, glycine addition increases the silicon oxide polishing removal rate to as much as 3 times over the standard process with no glycine addition.

[0055] As shown in Figure 7B, while the silicon oxide removal rate is enhanced with the addition of glycine, the silicon nitride removal rate is significantly suppressed. For the standard process, the average silicon nitride removal is 183 Å. In comparison, average removal for 3% and 6% glycine is 61 Å and 50 Å, respectively. This rate suppression effect is greatest at pH 10.5 and 6% glycine addition and the silicon nitride removal is measured to be only 5 Å.

[0056] Figure 7C shows the selectivity of silicon oxide to silicon nitride on blanket wafers. In Figure 7A-7C, the highest silicon oxide removal rate and the best silicon oxide to silicon nitride selectivity occur at pH 10.5 and 6% glycine. Under this condition, a silicon oxide to silicon nitride selectivity of 935:1 is seen compared to 16:1 for the standard process.

[0057] Based on the blanket wafer results, process conditions for DRAM patterned wafers are selected to determine the effect of the glycine addition on patterned wafer nitride loss during overpolish. DRAM STI patterned wafers (4200 Å HDP oxide, 950 Å LPCVD nitride, 150 Å pad oxide, 3800 Å trench) were chosen due to the availability of a well-established mask set. For each of three splits (pH 10.5 with 6% glycine, pH 10.5 and pH 12.0 without glycine) film thicknesses were measured after polishing for 30, 60, 120 and 180 seconds.

[0058] Figures 8A-8E demonstrate polishing results of DRAM wafers in one polishing process. Figures 8A-8B show the results from an Obsidian™ 8200C system. Figure 8A shows the remaining trench silicon oxide versus polishing time under different conditions. The thickness of the remaining trench silicon oxide material, such as the silicon oxide material 530 in Figures 6A-6B, was measured. The dashed line indicated as "clear oxide" represents the thickness of the trench oxide where the top surface of the trench silicon oxide is at the same height as the top surface of the silicon nitride layer, such as the silicon nitride layer 520 in Figures 6A-6B, and thus the silicon

oxide overfill is cleared. In Figure 8A, addition of glycine at pH 10.5 dramatically increases the silicon oxide removal rate. At a pH of 10.5 with no glycine, the silicon oxide polishing removal rate was significantly lower, the silicon oxide overfill was not cleared yet even after 180 seconds.

[0059] The silicon oxide clearing times and the calculated silicon nitride polishing removal rates are shown in Table 1. Comparison of the processes with pH 10.5 plus 6% glycine and pH 12.0 (no glycine) demonstrates that the process with glycine addition clears silicon oxide 12 seconds faster and has a 50% lower silicon nitride removal rate, leading to a significantly larger overpolish window. Presumably, the HDP silicon oxide peaks, as shown in the peaks 70 of Figure 1, or "hats" in the DRAM array activate the abrasive/binder matrix, liberating ceria during polishing. Once the wafer has been planarized and the topography removed, the silicon oxide removal rate drops dramatically.

Table 1. Split comparison

Split No.	Process	Time to Clear Oxide	Si_3N_4 Removal Rate
1	pH 10.5	180 sec	-
2	pH 10.5 + 6% glycine	30 sec	200 Å /min
3	pH 12.0	42 sec	384 Å /min

Table 2. DRAM3 polish summary for two treatments (averages)

	Oxide		Si_3N_4		
	WIW Range	WID Range	WIW Range	WID Range	Dishing
pH 12.0	578 Å	199 Å	453 Å	167 Å	128 Å
pH 10.5 + 6% glycine	186 Å	179 Å	311 Å	200 Å	210 Å

[0060] Figure 8B shows oxide within wafer (WIW) non-uniformity range versus polishing time. In Figure 8B, for 6% glycine, the silicon oxide WIW range does not show any degradation with overpolish. For the standard process, though, the silicon

oxide WIW range increases at a rate of about 300 Å/min of overpolish. Table 2 summarizes the results in comparing the planarization performance for splits 2 and 3. Comparison of dishing between the standard and glycine addition processes shows that the standard process performed better by an average of 82 Å. Within die (WID) non-uniformity range data did not indicate any significant effect of the glycine addition.

[0061] The results presented here demonstrate the ability to "stop on nitride" with silicon nitride blanket wafers and patterned DRAM wafers. By increasing the silicon oxide to silicon nitride selectivity, some degree of dishing performance is seen in Table 2. Use of very stiff low-compressibility subpads may be able to counteract this effect. In conjunction with the glycine addition, this may improve the WID uniformity and dishing without compromising the WIW uniformity. In general, the process with glycine addition clears silicon oxide faster than the standard process and shows a larger process window than the standard process for comparable oxide removal rate, insensitivity of WIW oxide range to wafer overpolish, and no significant impact on WID performance.

Example B:

[0062] Another example of an improved polishing process for a DRAM substrate is performed in an Applied Materials Inc. Reflexion™ CMP system using the 3M M3100 (SWR 159) fixed abrasive polishing pad on a 3M 6900 subpad.

[0063] Figures 8C-8E demonstrate polishing of DRAM wafers from a Reflexion™ system and show the overpolish and dishing results of the three treatments, pH 11.5, pH 10.5, and pH 10.5 with 6% glycine. Figure 8C shows nitride overpolish by comparing the remaining nitride versus additional polishing time. Figure 8D shows oxide overpolish by comparing the remaining trench oxide versus additional polishing time. After 120 second of overpolishing, about 400 Å of silicon nitride and about 600 Å trench silicon oxide are removed under the standard processes without the addition of any amino acid, and no additional silicon nitride removal and about 20 Å trench silicon oxide removal are demonstrated under the condition with the addition of 6% glycine at pH 10.5. Figure 8E shows dishing under different overpolish conditions. Dishing increases with overpolish time to about 15 times greater under the standard processes

without amino acid addition. Therefore, the stop-on-nitride capability is obtained by the glycine addition process, and the rate of dishing with overpolish is 80% lower for the process with glycine addition than for the standard process.

Example C:

[0064] Another example of an improved polishing process for DRAM STI patterned wafers involves a two-step, in-line polishing sequence performed on a Reflexion™ CMP system using the 3M M3100 (SWR 159) pad on a 3M 6900 subpad.

[0065] The two-step in-line polishing sequence includes pre-polishing of patterned wafers, followed by treatment with the processes and compositions described in this invention to demonstrate stop-on-nitride capability. The pre-polished wafers are already planarized, thereby eliminating the HDP topography as an aggressive activating factor leading to an undesirable silicon nitride removal rate on a M3100 pad. The thickness of the oxide remaining on the active areas is about 200 Å after completion of the first pre-polish step.

[0066] The intent of the 2-step in-line polishing sequence is to planarize the wafer on a first platen or a first step, removing the topography and the bulk of the oxide overfill, prior to a selective removal process on a second platen or a second step. The initial remaining silicon nitride thickness is about 850 Å after the first pre-polishing step. A stop-on-nitride process is demonstrated on a second platen with these less aggressive, blanket oxide-like wafers. Conditions for the three wafers polished by the in-line sequence are detailed in Table 3. All three wafers are processed similarly on platen 1. On platen 2, a glycine addition/no addition split is performed.

[0067] Figures 9A-9D demonstrate processing of DRAM wafers using such a polishing sequence. The thickness where the trench silicon oxide overfill is cleared to the same height as the top surface of the silicon nitride layer is indicated as "clear oxide". After polishing on platen 1, the wafers have approximately equal amounts of active-area trench silicon oxide remained before polishing on platen 2. Figure 9A shows remaining trench silicon oxide versus total polishing time on platen 2. Figure 9B shows remaining silicon nitride after polishing on platen 2. Wafer 1 and 2 show the

polishing results with glycine addition and less silicon nitride loss is observed for wafer 1 and 2 with glycine addition than wafer 3, where no glycine is added. Figures 9C and 9D demonstrate the remaining thickness profiles for the 3 wafers after polishing on platen 2 for 60 seconds and 160 seconds, respectively. Planarity results are shown in Table 4. WIW and WID performances are comparable for the two treatments. The glycine addition process shows slightly better silicon nitride ranges and the standard process shows slightly better silicon oxide ranges. Wafers polished in-line using the glycine addition just clear the silicon nitride. Without the glycine addition, polishing is shown to continue into the silicon nitride layer.

Table 3. In-line polishing conditions

DRAM wafers		Wafer 1	Wafer 2	Wafer 3
Platen 1				
	Cutting Fluid	pH 11.5	pH 11.5	pH 11.5
	Polish Time (sec)	20	20	20
Platen 2				
	Cutting Fluid	pH 10.5 + 6% glycine	PH 10.5 + 6% glycine	pH 10.5
	Polish Time (sec)	160	60	160

Table 4. DRAM3 wafer ranges

Wafer	Fluid	Si_3N_4 Removal (A)	SiN WIW (A)	SiN WID (A)	Ox WIW (A)	Ox WID (A)	Dishing (A)
1	pH 10.5 w/ 6% glycine	39	28	61	138	135	-23
2	pH 10.5 w/ 6% glycine	65	40	48	153	107	-28
3	pH 10.5 (standard)	184	54	85	142	70	-27

[0068] In conclusion, on a Reflexion™ CMP system, glycine addition continues to demonstrate capability of improving the fixed abrasive STI polishing process. In a single step polishing, aggressive activation of the abrasive by the HDP topography often result in a silicon nitride removal once the silicon oxide was cleared. Therefore, using an in-line polishing sequence, stop on nitride capability was demonstrated on DRAM3 wafers.

Example D:

[0069] Another example of an improved polishing process for logic applications is performed on a Reflexion™ CMP system using the 3M M3100 (SWR 159) pad on a 3M 6900 subpad. The addition of 6% glycine at pH 10.5 enhances silicon oxide removal and enables clearing of the nitride when polishing logic-type wafers with thicker oxide overfills.

[0070] Historically, the 3M M3100 (SWR159) pad has had trouble successfully polishing logic wafers. Previous attempts are highlighted by an inability to clear the large features and a tendency to severely overpolish the small features. Because of the silicon oxide removal rate enhancement and silicon nitride removal rate suppression effects, glycine addition may enable logic applications for a fixed abrasive pad, such as the 3M M3100 pad.

[0071] MIT 964 patterned wafers were used as standardized proxy logic wafers. The process conditions for one such wafers, wafer 12, are shown in Table 5. The results for one such wafer, wafer 12, are shown in Figures 10A and 10B. On the M3100 pad without glycine addition, polishing conditions are pushed to the edge of the process window for wafer 12, as shown in Table 5, yet the silicon nitride did not clear over the large high-density features. Figure 10A shows remaining nitride versus wafer diameter of wafer 12 for a standard process without glycine addition, which results in strong low frequency vibrations throughout the process and over-polish of the small low-density areas.

Table 5. Wafer 12 process conditions

Tape incr (mm)	20	Polish Time (sec)	240	Cutting Fluid	DIW + KOH
Pad	3M SWR 159	P_{IT} / P_{RR} / P_{mem} (psi)	1/6.8/5.5	PH	12.0
Subpad	3M 6900	S_{platen}/ S_{head} (rpm)	33/31	Flow rate (ml/min)	400

[0072] Figure 10B shows remaining trench oxide versus wafer diameter and compares wafer 12 with a wafer polished using a two-step in-line polishing approach. In the two-step sequence, the main polishing step switches to a lower pressure during second step with the intention of reducing the polishing aggressiveness and allowing the process to stop on nitride. The 2 step polishing conditions are shown in Table 6.

Table 6. Two step polishing recipe

	Time (sec)	Pressure (psi)	Speed (rpm)
Step 1	30	1/6.8/5	33/31
Step 2	150	1/2.5/2	33/31

[0073] The silicon nitride is cleared on wafer 12 but the small low-density areas are still over-polished. No notable vibrations are experienced while polishing with the two-step in-line polishing approach plus glycine addition. On the 3M M3100 pad, the silicon oxide removal rate enhancement by adding glycine enabled polishing of logic-type wafers. The results demonstrate that the addition of glycine enables planarization of logic-type wafers with fixed abrasive CMP.

[0074] The above-specified components and processing parameters are illustrative and should not be construed as limiting the invention. It is contemplated that the compounds and concentrations used may be varied to provide desired removal rates of 100 Å/min or higher, desired selectivity to stop-on-planar, desired selectivity to stop-on-nitride, and the nature and amount of the desired materials to be removed from the substrate surface. As an example, Steps 210, 220, and 230 in Figure 3 may be performed as part of one continuous operation, or two or more distinct operations. For

example, the invention contemplates that different steps may be performed on one or more platens, or portions of some process steps may be performed on different platens.

[0075] While the foregoing is directed to embodiments of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.